
DESIGN AND IMPLEMENTATION OF SYNCHRONOUS DC-DC BUCK CONVERTER

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ABSTRACT

This paper introduces the synchronous dc-dc buck converters design, implementation and simulation. With high efficiencies of synchronous converter instead of using a traditional converter. It presents the theoretical derivations and parameters equations with design and Simulation results for the proposed synchronous buck converter. The mathematical model for the synchronous buck converter is analyzed through the theoretical equation, simulated with MATLAB SIMULINK and implemented using the designed components. The output of the Buck converter depends on four aspects; selected frequency, inductor value, capacitor value, and type of MOSFETs, which represented in this work.

KEYWORDS: DC-DC Buck converter, syn,, Multi-junction solar cells, High efficiency.

BACKGROUND

Control of electric power could be done by converting the electric power from to another which is the core of the nowadays technology, that is used in many applications like motherboards, solar array MPPT control technique, motors control in electronic automobiles, marine hoists, trolley cars, and forklift trucks... etc. The widely usage of dc – dc buck converters is due to providing smooth acceleration control, high efficiency, and fast dynamic response . This conversion could be done by using static power converters . There are many types of converters, many applications can be widely used the Dc–Dc buck converters such as

- Convert a dc input voltage into a dc output voltage.
- Regulate the dc output voltage against load and line variations.
- Reduce the ac voltage ripple on the dc output voltage below the required level.
- Provide isolation between the input source and the load (isolation is not always required).
- Protect the supplied system and the input source from electromagnetic interference (EMI).

There are two main types of dc–dc converters; linear power regulators whose principle of operation is based on a voltage or current divider which are inefficient. The other type is switching regulators which use power electronic semiconductor switches in ON and OFF states. Which reduce the power losses in those states and increase the efficiencies, switching regulators can achieve high energy conversion efficiencies. The switching dc–dc converters can be divided into two main types; Soft-switching converters (resonant converters), and Hard-switching pulse width modulated (PWM) converters.

Soft-switching converters is called resonant converters which is used for resonant network dc-dc conversion, the switching losses in the semiconductor device are avoided Compared to the PWM converters in the resonant converters due to the fact that the current through or voltage across the switching device is at the switching point is equal to or near zero and also decrease the harmonic content in the converter voltage and current waveforms. Hard-switching, it is called also pulse width modulated (PWM) converters, and it needs high efficiency, constant frequency operation, relatively simple control and commercial availability of integrated circuit controllers, and ability to achieve high conversion ratios for both step-down and step-up application. On the other hand, the PWM dc–dc converters (due to the switching of semiconductor devices normally occurs at high current levels) is that PWM rectangular voltage and current waveforms cause turn-

on and turn-off losses in semiconductor devices which limit practical operating frequencies to a megahertz range.

There are three types of PWM switching regulators; Buck regulator (step down), Boost regulator (step up), and Buck-boost regulator(step up and step down). The boost is one of the fundamental switch-mode power topologies. The other being is the buck regulator. From these two topologies, all other topologies switch-mode power supply topologies are derived.

DC-DC BUCK & SYNCHRONOUS CONVERTER

A buck converter consists of dc input voltage source, V_{in} , controlled switch, Q1 (MOSFET), controlled switch (diode D1), filter inductor, L1, filter capacitor, C_{out} , and load resistance, R_L . The input is exposed to the switch Q1. An input capacitor C_{INP} is required to filter the input current into the converter because the input current is a highly dynamic waveform.



Figure 1: basic & synchronous buck dc- dc converter circuit.

The dc- dc converter has two modes of conductions; Continuous Conduction Mode (CCM) where Inductor current remains positive throughout the switching period, and Discontinuous Conduction Mode (DCM) where Inductor current remains zero for some time in the switching period. figure (2) shows different conduction modes.

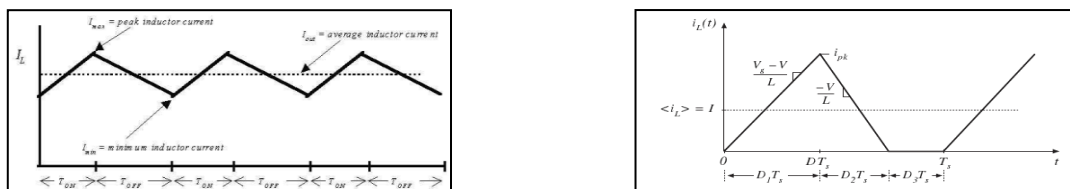


Figure 2: The dc- dc converter has two modes of operation.

ON mode: When switching element Q1 is ON (is closed), current flows from VIN through the inductor L linearly rises and charges the output smoothing capacitor C_o , the voltage across the inductor is $V_L = V_i - V_o$. and the output current I_o is supplied. The current which flows into the coil L at this time induces a magnetic field, and electric energy is transformed into magnetic energy and accumulated for storage. The diode doesn't allow current to flow through it, since it is reverse-biased by voltage .

OFF mode: When switching element Q1 is OFF (is opened), free-wheeling diode D turns ON (forward biased) and energy stored in L is then released to the output side. the voltage across the inductor is $V_L = -V_o$. The inductor current which was rising in ON case now decreases until transistor Q1 is switched on again in the next cycle.

DESIGN METHODOLOGY OF SYNCHRONOUS CONVERTER

The design of dc-dc converters require proper selection of the values of converter components like inductor, capacitor, transistor, diode and switching frequency. This is important to decide the converter efficiency, performance and the output characteristics

Operating frequency: which determines the performance of the switch. The higher is the switching frequency, the smaller the physical size and value of the capacitor and inductor. At higher frequencies the switching losses in the MOSFET increase, and therefore reduce the overall efficiency of the circuit so switching frequency selection is normally determined by efficiency requirements. On the other hand, the trade-off between size and efficiency has to be evaluated carefully.

Inductor sizing and Selection: controls the percent of the ripple current that the inductance is inversely proportional to the ripple current and also determines whether or not the circuit is operating in the continuous mode. The peak current through the inductor is used to determine the inductor's required saturation current rating, which in turn commands the approximate size of the inductor.

A smaller inductor value enables a faster transient response; it also results in larger current ripple, which causes higher conductor losses in the switches, inductor, and parasitic resistances. The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple. On the other hand, Critical inductance L_c is the minimum value of the inductor for a given D , f and R before the converter enter the discontinuous conduction mode (DCM) of operation.

Critical inductance calculation

$$L = \frac{V_o (V_{in} - V_o)}{F V_{in} \Delta I} = \frac{V_{in} D (1 - D)}{F \Delta I} = \frac{D (V_{in} - V_o)}{F \Delta I}$$

$$L_c = \frac{(1 - D_{max})}{2F} R_{max}$$

$$I_{L-max} = I_L + \frac{\Delta I}{2}$$

$$I_{L-min} = I_L - \frac{\Delta I}{2}$$

Where:

D_{max} : Calculated at Minimum Input Voltage

R_{max} : Calculated at Minimum Output Current , $R_{max} = V_o/I_{o-min}$

- I_{o-min} is either given as percentage of load to maintain CCM, e.g. 10% load with CCM
- Or, I_{o-min} is calculated as specified by maximum Δi_L , such that $I_{o-min} = \Delta i_L/2$

F : Switching frequency normally chosen by the designer, the higher the switching frequency, the smaller the required critical inductance, i.e. beneficial for reducing size of Buck.

Inductor Peak current calculation

At Worst case maximum inductor current occurs at maximum load which causes Maximum output power rating per specified required output voltage

$$V = L * \Delta I / \Delta T$$

$$L = (V_{in} - V_{out}) * \left(\frac{D}{F_{sw}}\right) / I_{ripple}$$

$$L = 7 * (0.416/400) / 0.6 = 12.12 \mu H$$

$$I_{L-max} = I_L + \frac{\Delta I_L}{2} = V_o \left[\frac{1}{R_{min}} + \frac{[1 - D_{min}]}{2LF} \right]$$

OUTPUT CAPACITOR SELECTION

The output filter capacitors are chosen to meet an output voltage ripple specifications, as well as the ability to handle the required ripple current stress. The primary criterion for selecting the output filter capacitor is its

capacitance and equivalent series resistance, ESR. Since the capacitor's ESR affects the efficiency, low ESR capacitors will be used for best performance. For reducing ESR, it is possible to connect few capacitors in parallel. The critical capacitance calculation:

Assume $ESL=0$

$$\Delta V = \Delta I * (ESR + \frac{\Delta T}{C})$$

$$C = \frac{\Delta I * \Delta T}{(\Delta V - (\Delta I * ESR))}$$

$$C_{out} = (0.6 * 1.04) / (0.05 - (0.6 * 0.3))$$

$$C_{out} = 19.5 \mu F$$

$$C_c = \frac{V_o (1 - D_{min})}{8 * L * F^2 * \Delta V_{LO}}$$

RMS current rating calculation:

$$i_{c-rms} = \frac{V_o (1 - D_{min})}{2\sqrt{3} * L * F}$$

Voltage Rating: Capacitor Voltage should withstand with the maximum output voltage

$$V_{C-max} = V_o + \frac{\Delta V_o}{2}$$

The electrolytic capacitors are polarized capacitors because of their anodization principle. They can only be operated with DC voltage applied with the correct polarity. Operating the capacitor with wrong polarity or with AC voltage leads to short circuit and can destroy the component.

INPUT CAPACITANCE CALCULATION

$$I_{ripple} = \frac{I_{LOAD}}{2} = 1 \text{ amp}$$

$$\text{Assume } V_{ripple} = 200 \text{ mv}$$

$$\text{Capacitor ESR} = 0.12 \text{ ohm}$$

$$C = \frac{\Delta T}{(V_{ripple} / I_{ripple}) - (ESR)} = 13 \mu F$$

$$C_{in} = \frac{I_{O-max} * D * (1 - D)}{f * \Delta V_{in}}$$

DIODE SELECTION

The ON duration of the diode is : (1 - duty cycle)

Voltage rating:

- With ideal switch, the $VRRM = V_{in-max}$
- For non-ideal diode, $VRRM = V_{in-max} + V_{SW}$ where V_{SW} is the maximum forward drop across the switch (calculated at maximum load current)

Current rating:

$$I_F > I_{O-max} * (1 - D_{min})$$

The selected diode is 6.0 AMPS, silicon rectifier, (type number 6A4M or 6A40). Electrical features, low forward voltage drop ($V_f\text{-max} = 1.1\text{V}$), high current capability ($I_f\text{-max} = 6\text{ A}$), high reliability and high surge current capability

$$I_D = (1 - D) * I_{LOAD}$$

$$I_D = (1 - 0.416) * 2 = 1.174$$

MOSFET SELECTION:

Voltage rating:

- With ideal diode, the $V_{\text{switch-max}} = V_{\text{in-max}}$
- For non-ideal diode, $V_{\text{switch-max}} = V_{\text{in-max}} + V_F$ where V_F is the maximum forward drop across the diode (calculated at maximum load current)

Current rating:

- Switch current rating is calculated based on average value
- By KCL, Inductor Current = Switch Current + Diode Current
- During tON, Inductor current equals switch current
- During tOFF, Inductor current equals diode current

$$I_{sw\text{-max}} > I_{o\text{-max}} * D_{max}$$

Assume -30V, -9.3 amp Mosfet for low R_{ds} (0.02 ohm)

$$P_{conduction} = I_D^2 * R_{ds} * D = 2 * 2 * 0.02 * 0.416 = 0.033 \text{ watt}$$

$$P_{switching} = \left(V * \frac{I_D}{2} \right) * (T_{on} + T_{off}) * F_{sw} + (C_{oss} * V^2 * F_{sw}) = ((7 * 2/2) * 100\text{nsec} * 400\text{Khz}) + (890\text{pf} * 7 * 7 * 400) = 0.28 + 0.017 = 0.297 = 0.3 \text{ watt}$$

Design specifications:

Parameters	Value
Input voltage range V_{in}	12V
Output voltage V_{out}	5V
Input ripple voltage ΔV_{in}	0.3
Output ripple voltage ΔV_o	0.2V
Max Output current I_o	2A
Inductor ripple current ΔI_L	3.6A (30% of output rating current)
Percent minimum load-CCM	10% of maximum power (1.2A)
Switching frequency f_{sw}	400KHz
RL	2.333 to 23.333
Duty cycle V_{in}/V_{out}	0.416

BUCK CONVERTER EFFICIENCY:

The efficiency determination is an important factor in the design of the DC-DC converter.

The losses due to Buck components are:

1. Inductor's copper loss

2. Capacitor's ESR loss
3. Static loss of MOSFET
4. Switching loss of MOSFET
5. MOSFET Gate Drive Losses
6. Static loss of diode
7. Switching loss of diode

Inductor copper Loss Considerations

$$P_{LO} = I_{o,max}^2 \times R_{LDC}$$

$$P_{LO} = 12^2 \times 0.0147 = 0.15W$$

From a catalog, a 120 μ H, 12 amp inductor has a resistance of (0.0147) ohm

Output capacitors ESR Loss Considerations

$$P_{Co-ESR} = I_{o,max}^2 \times ESR$$

$$P_{Co-ESR} = 12^2 \times 0.034 = 0.01W$$

Input capacitors ESR Loss Considerations

$$P_{Cin-ESR} = I_{o,max}^2 \times ESR$$

$$P_{Cin-ESR} = 12^2 \times 0.055 = 0.12W$$

MOSFET LOSS CONSIDERATIONS

Selecting a particular MOSFET for this design requires a power loss analysis. There are two main power losses associated with the MOSFET. The first is the power loss due to the current flowing through the small internal resistance of the MOSFET when the switch is closed (The ON resistance of MOSFET R_{DSon}). The ON resistance of MOSFET R_{DSon} has directly effect on the static loss, and mainly it depends on the applied gate voltage and temperature of the MOSFET

The second is the power loss during the rise and fall times of the switch. The power losses due to switching speed and internal resistance must be combined

1- Static loss of MOSFET

$$P_{static} = I_{o-max}^2 * R_{DS-on} * D_{max}$$

$$P_{static} = 12^2 \times 0.075 \times 0.9333 = 0.3W$$

2- Switching loss of MOSFET

$$P_{switching} = \left(\frac{1}{6}\right) I_{o-max} * V_{in-max} * f_{sw} (t_{d-on} + t_{d-off}) + (1/2) V_{in}^2 * C_{oss} * f_{sw}$$

$$P_{switching} = \left\{ \left(\frac{1}{6}\right) \times 12 \times 40 \times 100 \times 10^3 \times (14 + 41) \times 10^{-9} \right\}$$

$$+ \left\{ \left(\frac{1}{2}\right) \times 315 \times 10^{-12} \times 40^2 \times 100 \times 10^3 \right\}$$

$$\left\{ \left(\frac{1}{2}\right) \times 315 \times 10^{-12} \times 40^2 \times 100 \times 10^3 \right\} = 0.4652W$$

Diode Loss Considerations

$$P_{VFD} = V_F \times I_{O-max} \times (1 - D_{min})$$

$$P_{VFD} = 0.85 \times 12 \times (1 - 0.7) = 0.47W$$

DC-DC buck Converter efficiency

$$\eta = \frac{P_{out}}{P_{out} + P_{total-loss}} = \frac{10}{10 + 1.05} = 90.5\%$$

Gate Drive Losses of MOSFET

$$P_{conduction} = I_D^2 * R_{DS-on} * (1 - D_{max}) = 2 * 2 * 0.0044 * (1 - 0.416) = 0.01watt$$

$$P_{gate} = (1/2) V_{GS} * Q_{gate} * f$$

$$P_{gate} = \left(\frac{1}{2}\right) \times 123 \times 10^{-9} \times 5 \times 100 \times 10^3 = 0.03075W$$

Synchronous Converter efficiency (proposed system)

$$\eta = \frac{P_{out}}{P_{out} + P_{total-loss}} = \frac{10}{10 + 0.59} = 94.4\%$$

In the synchronous topology the low-side MOSFET's lower resistance from drain to source (RDSON) helps reduce losses significantly and therefore optimizes the overall conversion efficiency. However, all of this demands a more complicated MOSFET drive circuitry to control both the switches. Care has to be taken to ensure both MOSFETs are not turned on at the same time. If both MOSFETs are turned on at the same time a direct short from VIN to ground is created and causes a catastrophic failure. Ensuring this direct short, which is also called cross-conduction or shoot-through, does not occur requires more complexity and cost within the IC.

MATLAB SIMULATION RESULTS OF SYNCHRONOUS DC-DC CONVERTERS

The simulation of the buck converter is accomplished using Matlab/Simulink and the simulation results are presented in this section as follows.

Firstly, at duty ratio (0.5) and three different values of load resistance , an input voltage (40V). The output voltage, the inductor current and the load current are

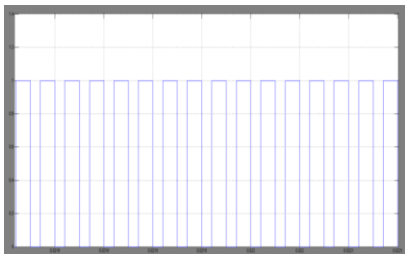


Figure 3: shows that the Pulse Width Modulation Signals PWM1 .

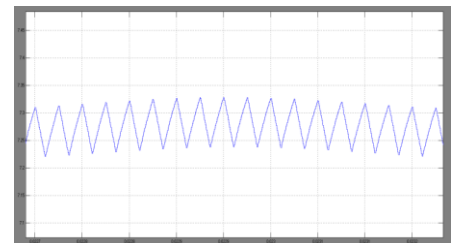


Figure 5: Zoom in of the Output Voltage (V)

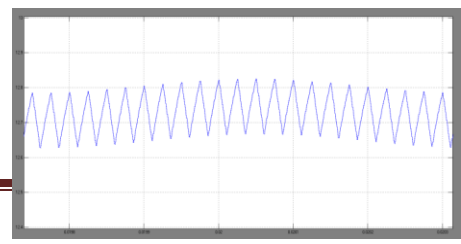


Figure 4: shows that the input Voltage of the System,



Figure 6: Zoom in of the Output Current (Amp)

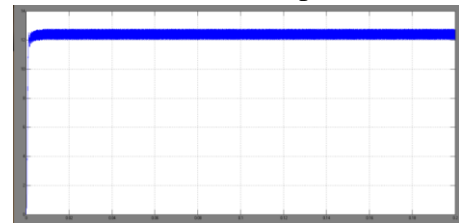


Figure 7: shows that Output Voltage wave form of the Closed Loop System

CONCLUSIONS

From this paper proposes a synchronous buck converter controlled by PWM signals designed for pv system. Its simulated in matlab Simulink ,the results show that its more better than conventional converter that suppose to be a perfect choice in the autonomous systems because the main advantage of the synchronous converter having fixed constant output voltage that improve the efficiency of the photovoltaic system with better energy transformation The peak power conversion efficiency is measured to be more than 90%, whereas the MPPT accuracy is greater than 94%, which fulfills the design objective

By replacing the rectifier diode D1 with a MOSFET Q2, operated as a synchronous rectifier (SR), the equivalent forward-voltage drop can be lowered and the corresponding conduction loss reduced. This is due to the fact that the low on-resistance property of the SR MOSFET reduces Ohmic losses. However, at higher currents, the drop across the MOSFET's on-resistance can exceed that of a diode. This limitation, however, is normally addressed by paralleling two or more SR MOSFETs. In applications where the current requirement is very high more than 32 A, paralleling two SR MOSFETs can further reduce the on-resistance and corresponding losses. Such paralleling is not practical with rectifier diodes of nonsynchronous topology.

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